AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth below. A listing of all pending claims is presented below.

1. (Original) A data reading method in a semiconductor memory device, said semiconductor memory device having a memory cell that stores data by state of polarization of a ferroelectric capacitor, said data reading method comprising:

a first reading step for applying a first reading pulse to said memory cell to generate a first signal corresponding to the stored data;

a writing step for writing reference signal generating data corresponding to a signal on a high level side to said memory cell;

a second reading step for applying a second reading pulse to said memory cell to generate a second signal corresponding to said reference signal generating data;

a reference signal generating step for generating a reference signal on a basis of said second signal; and

a determining step for comparing said first signal with said reference signal, and determining said stored data stored in said memory cell.

2. (Original) A data reading method as claimed in claim 1,

wherein in said first reading step and said second reading step, said first signal and said second signal are generated using a remaining signal after said reading pulse applied is returned from a high level to a low level.

3. (Original) A data reading method as claimed in claim 1,

wherein said semiconductor memory device further includes switch means disposed between said memory cell and a constant-voltage node; and

in said writing step, the reference signal generating data corresponding to the signal on the high level side is written to said memory cell by making said switch means conduct.

4. (Original) A data reading method as claimed in claim 1,

wherein in said reference signal generating step, said reference signal is generated according to said second signal by converting said second signal to substantially 1/2.

5. (Original) A data reading method as claimed in claim 1,

wherein said first signal and said second signal are generated according to a potential change occurring in a load capacitance, and in said reference signal generating step, said reference signal is generated by distributing said second signal to a load having a substantially identical capacitance.

6. (Original) A data reading method as claimed in claim 1,

wherein said semiconductor memory device has a cell string configuration in which one terminal of each of a plurality of said memory cells is connected to a common node electrode;

said first signal and said second signal are generated according to a potential change occurring at said common node electrode; and

in said reference signal generating step, said reference signal is generated by short-circuiting said common node electrode and a common node electrode of an adjacent cell string

and converting said second signal occurring at said common node electrode to substantially 1/2.

7. (Original) A data reading method in a semiconductor memory device, said semiconductor memory device including: a plurality of memory cells for passing a current corresponding to stored data through a bit line when selected to be read; a current supplying transistor disposed between said bit line and a constant-voltage node; and switch means disposed between a gate of said current supplying transistor and said bit line, said data reading method comprising:

a first reading step for short-circuiting the gate of said current supplying transistor and the bit line, and performing a first reading from said memory cell;

a second reading step for disconnecting the gate of said current supplying transistor from the bit line, and performing a second reading from said memory cell; and

a determining step for determining said stored data stored in said memory cell according to a potential state of the bit line, said potential state occurring in said second reading step.

8. (Canceled)

9. (Canceled)

10. (Original) A semiconductor memory device comprising:

a memory cell for storing data by state of polarization of a ferroelectric capacitor;

reading means for selectively applying a reading pulse to said memory cell to generate a signal corresponding to the stored data, and applying a first reading pulse and a second reading

pulse in one reading operation to said memory cell;

writing means for, after said reading means applies the first reading pulse to the selected memory cell and a first signal corresponding to the stored data of the selected memory cell is generated, writing reference signal generating data corresponding to a signal on a high-level side to the selected memory cell before said reading means applies the second reading pulse;

reference signal generating means for generating a reference signal on a basis of a second signal generated by applying said second reading pulse and corresponding to said reference signal generating data stored in said selected memory cell; and

determining means for comparing said first signal with said reference signal, and determining said stored data stored in said memory cell.

11. (Original) A semiconductor memory device as claimed in claim 10,

wherein said reading means generates said first signal and said second signal using a remaining signal after said reading pulse applied is returned from a high level to a low level.

12. (Original) A semiconductor memory device as claimed in claim 10, further comprising switch means disposed between said memory cell and a constant-voltage node,

wherein said writing means writes the reference signal generating data corresponding to the signal on the high level side to said memory cell by making said switch means conduct.

13. (Original) A semiconductor memory device as claimed in claim 10,

wherein said reference signal generating means generates said reference signal according to said second signal by converting said second signal to substantially 1/2.

14. (Original) A semiconductor memory device as claimed in claim 10,

wherein said first signal and said second signal are generated according to a potential change occurring in a load capacitance, and said reference signal generating means generates said reference signal by distributing said second signal to a load having a substantially identical capacitance.

15. (Original) A semiconductor memory device as claimed in claim 10,

wherein a plurality of said memory cells have a cell string configuration in which one terminal of each of the plurality of said memory cells is connected to a common node electrode;

said first signal and said second signal are generated according to a potential change occurring at said common node electrode; and

said reference signal generating means generates said reference signal by short-circuiting said common node electrode and a common node electrode of an adjacent cell string and converting said second signal occurring at said common node electrode to substantially 1/2.

16. (Original) A semiconductor memory device comprising:

a plurality of memory cells connected to a bit line;

reading means for reading a selected memory cell, and passing a current corresponding to data stored in said selected memory cell through said bit line;

a current supplying transistor disposed between said bit line and a constant-voltage node;

switch means disposed between a gate of said current supplying transistor and said bit line; and

determining means for, when said reading means performs a first reading of the selected memory cell in a state in which the gate of said current supplying transistor and the bit line are short-circuited and then said reading means performs a second reading of the selected memory cell in a state in which the gate of said current supplying transistor and the bit line are disconnected from each other, determining the stored data stored in said selected memory cell according to a potential state of the bit line, the potential state being produced by said second reading.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)